CLAIMS

1. A three-dimensional device comprising a plurality of thin film device layers deposited in a thickness direction, each thin film device layer being disposed in a predetermined region in a planar direction, wherein at least one of the thin film device layers is deposited by a transfer method.

2. A three-dimensional device comprising a plurality of thin film device layers deposited on a base in a thickness direction for constituting a three-dimensional circuit, each thin film device layer constituting a circuit disposed in a predetermined region extending in a planar direction, wherein at least one of the thin film device layers is deposited by a transfer method.

3. The three-dimensional device according to one of claims 1 and 2, wherein the transfer method comprises the steps of forming a thin film device layer on a support substrate with a separable layer therebetween, and irradiating the separable layer with light to cause a separation in the separable layer and/or at an interface so that the thin film device layer on the support substrate is transferred to a substrate of the three-dimensional device.

4. The three-dimensional device according to claim 3, wherein the separation of the separable layer is caused by breakage or weakening of interatomic or intermolecular bonds in a material constituting the separable layer.

5. The three-dimensional device according to claim 3, wherein the separation of the separable layer is caused by evolution of gas from a material constituting the separable layer.

6. The three-dimensional device according to claim 3, wherein the light is a laser beam.

7. The three-dimensional device according to claim 3, wherein the separable layer comprises any one of amorphous silicon, ceramic, metal, and organic polymeric material.

8. The three-dimensional device according to one of claims 1 and 2, wherein the thin film device layer comprises connecting electrodes, the connecting electrodes electrically connecting two adjacent thin film device layers to each other.

9. The three-dimensional device according to claim 8, wherein the connecting electrodes are provided on both surfaces of the thin film device layer.

10. The three-dimensional device according to claim 8, wherein two adjacent thin film device layers are joined to each other with an anisotropic conductive film therebetween.

11. The three-dimensional device according to one of claims 1 and 2, wherein in two selected layers of the thin film device layers, one layer has a light-emitting section and the other layer has a light-receiving section, the light-emitting section and the light-receiving section enabling optical communication between the two layers.

12. The three-dimensional device according to one of claims 1 and 2, wherein the thin film device layer deposited by transferring is formed simultaneously with at least one of the other thin film device layers.

13. The three-dimensional device according to one of claims 1 and 2, wherein at least one of the thin film device layers comprises a plurality of thin film transistors.

14. The three-dimensional device according to one of claims 1 and 2, wherein at least one of the thin film device layers comprises a memory cell array.

15. The three-dimensional device according to one of claims 1 and 2, wherein a plurality of layers among the thin film device layers comprise one memory.

16. The three-dimensional device according to one of claims 1 and 2, wherein at least one of the thin film device layers comprises a memory cell array, and at least one of the other thin film device layers comprises a logic circuit.

17. The three-dimensional device according to claim 16, wherein the logic circuit drives the memory cell array.

18. The three-dimensional device according to claim 16, wherein the logic circuit and the memory cell array are formed in accordance with different design rules.

19. The three-dimensional device according to claim 16, wherein the logic circuit and the memory cell array are formed in accordance with different design parameters.

20. The three-dimensional device according to claim 16, wherein the logic circuit and the memory cell array are formed by different fabricating processes.